

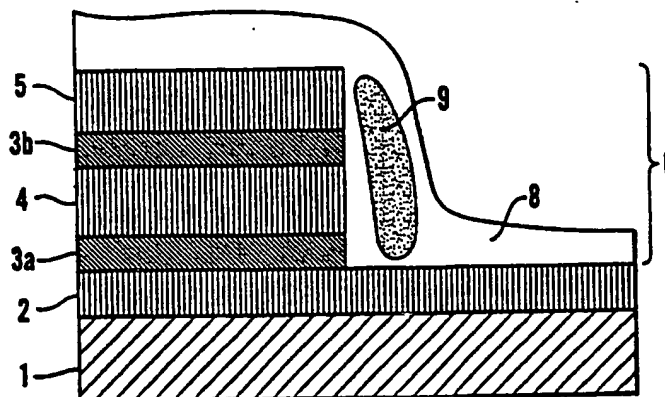
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<p>(21) International Application Number: PCT/NO99/00013</p> <p>(22) International Filing Date: 14 January 1999 (14.01.99)</p> <p>(30) Priority Data:</p> <table border="0"> <tr> <td>980224</td> <td>16 January 1998 (16.01.98)</td> <td>NO</td> </tr> <tr> <td>985472</td> <td>23 November 1998 (23.11.98)</td> <td>NO</td> </tr> </table> <p>(71) Applicant (for all designated States except US): OPTICOM ASA [NO/NO]; Brynsveien 3B, N-0667 Oslo (NO).</p> <p>(72) Inventors; and</p> <p>(75) Inventors/Applicants (for US only): BERGGREN, Rolf, Magnus [SE/SE]; Vasavägen 30, S-582 33 Linköping (SE). GUSTAFSSON, Bengt, Göran [SE/SE]; Trumslagaregatan 33, S-582 16 Linköping (SE). KARLSSON, Johan, Roger, Axel [SE/SE]; Stenhogsvägen 168, S-589 27 Linköping (SE).</p>	980224	16 January 1998 (16.01.98)	NO	985472	23 November 1998 (23.11.98)	NO	<p>(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published</p> <p><i>With international search report.</i></p> <p><i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p> <p><i>In English translation (filed in Norwegian).</i></p>
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(54) Title: A FIELD-EFFECT TRANSISTOR



(57) Abstract

A field-effect transistor is made with electrodes (2, 4, 5) and isolators (3) in vertically provided layers, such that at least the electrodes (4, 5) and the isolators (3) form a step (6) oriented vertically relative to the first electrode (2) or the substrate (1). Implemented as a junction field-effect transistor (JFET) or a metal-oxide semiconducting field-effect transistor (MOSFET) the electrodes (2, 5) forming respectively the drain and source electrode of the field-effect transistor or vice versa and the electrode (4) the gate electrode of the field-effect transistor. Over the layers in the vertical step (6) an amorphous, polycrystalline or microcrystalline inorganic or organic semiconductor material is provided and forms the active semiconductor of the transistor contacting the gate electrode (8) directly or indirectly and forming a vertically oriented transistor channel (9) of the p or n type between the first (2) and the second (5) electrode. In a method for fabrication of a field effect transistor a vertical step (6) is formed by a means of a photolithographic process and a soluble amorphous active semiconductor material (8) is deposited over the first electrode (2) and the vertical step (6) such that a vertically oriented transistor channel between the drain and source electrode (2, 5) is obtained. In a JFET the semiconductor material (8) contacts the gate electrode (4) directly. In a MOSFET a vertically oriented gate isolator (7) is provided between the gate electrode (4) and the semiconductor material (8).

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A field-effect transistor.

The present invention concerns field-effect transistors, respectively a junction field-effect transistor and a metal-oxide semiconductor field-effect transistor (MOSFET) with substantially vertical geometry, wherein the field-effect transistors comprise a planar substrate of non-conductive material. The invention also concerns a method for fabrication of field-effect transistors of this kind with a substantially vertical geometry, wherein the transistor comprises a planar substrate of non-conducting material.

Field-effect transistors (FET) which use an amorphous material as the active semiconductor are traditionally realized in a horizontal geometry such as rendered in fig. 1 which shows two examples (fig. 1a, fig. 1b) of the realization of a thin-film field-effect transistor according to prior art. Here the drain electrode and the source electrode are mutually separated by a transistor channel. This channel consists of an amorphous semiconductor material. The gate electrode is defined as a horizontal layer which is isolated from the channel by means of the gate isolator. The transistor effect is defined either as a depletion mode or an enrichment mode, depending on the gate potential. As the active amorphous semiconductor material in field-effect transistors of this kind conjugated polymers, aromatic molecules, and amorphous inorganic semiconductors have been used. For instance fig. 1 shows a thin-film transistor with an active semiconductor material in the form of amorphous Si:H in a 10 nm thick layer (D.B. Thomasson & al., IEEE El. Dev. Lett., Vol. 18, p. 117; March 1997). A gate electrode which may be of metal, is provided on a substrate. An isolating layer of silicon nitride (SiN) is provided over this gate electrode and the active semiconductor material in form of amorphous Si:H is provided over the isolator in a 10 nm thick layer. The drain electrode and the source electrode are provided mutually spaced apart on the active semiconductor material. They are realized in a different metal than the gate electrode, for instance aluminium. Another example of an organic thin film transistor is shown in fig. 1b (A. Dodabalapur & al., Appl. Phys. Lett.; Vol. 69, pp.4227-29, December 1996). Here the active semiconductor material is an organic compound, for instance a polymer or aromatic molecules. As in the example in fig. 1a the gate electrode is provided on a substrate and above the gate electrode an isolator is provided in the form of a layer which may be made by coating the surface of the gate electrode with an oxide layer, something which may be

realized by oxidizing the material in the surface of the gate electrode. The source and drain electrode are provided spaced apart on the isolating layer and spaced apart vertical side walls which on one end are mutually connected with a similar vertical transverse wall are provided over the drain and source electrode. In the plane perpendicular to the walls the transistor channel hence obtains a section formed as a U, where the side walls are the legs of the U and the transverse wall the crossline. The layers may be provided standing on a suitable substrate and wholly covered by a layer of isolating material. Over the isolating layer a conducting layer is provided, forming the gate electrode of the transistor. The ends of the side walls or the ends of the legs of the U shaped channel structure are exposed and in these end areas of the channel the source and drain electrodes respectively are formed, for instance by an ion implantation process. The primary object of a thin-film transistor of this kind is to provide a satisfying channel length on a smaller area than can be obtained with more conventional embodiments, while the stray current is reduced when the transistor is in an off-state.

Fig. 1c shows a schematically and in principle a planar JFET structure according to prior art, in this case realized as an n-channel JFET.

The use of an amorphous semiconductor material makes possible the realization of different transistor geometries if the very special processing properties of the amorphous materials are exploited. The object of the present invention is hence to provide a field-effect transistor, respective a junction field-effect transistor (JFET) and a metal-oxide field-effect transistor (MOSFET) with vertical geometry and even more particular the object is to deposit the amorphous active semiconductor material in the form of organic molecules, a conjugated polymer or an amorphous inorganic semiconductor on a vertical structure which comprises both the gate electrode and either the drain electrode or the source electrode. Finally it is also an object to provide a vertically oriented transistor channel.

Common semiconductor devices have formerly been made with vertical geometry. The purpose of this is a more effective exploitation of the chip area. A transistor with vertical geometry is expected to require less space than a transistor with horizontal geometry.

For instance it is from US patent nr. 5 563 077 (H.C. Ha) known a thin-film transistor with a vertical channel, wherein the channel is formed with two

mutually spaced apart vertical side walls which at one end are connected with a similarly vertical end-wall. In the plane perpendicular to the walls the transistor channel hence obtains a U-shaped section, wherein the side walls are the legs of the U and the end wall the cross line. The walls may be
5 provided on a suitable substrate and wholly covered by a layer of isolating material. A conducting layer which forms the gate electrode of the transistor is provided over the isolating layer. The ends of the side walls or the end of the U-shaped channel structure is exposed and on these end areas of the
10 channel the source and drain electrodes respectively are formed, e.g. by means of an ion implantation process. The primary object of a thin film transistor of this kind is to provide a satisfying channel length on a smaller area than that which may be obtained with more conventional embodiments, while the leakage current is reduced when the transistor is in off-state.

The above-mentioned objects and other advantages are achieved according to
15 the invention with a junction field-effect transistor (JFET) which is characterized in that a layer of conducting material which comprises a first electrode is provided on the substrate that a layer of isolating material which forms a first isolator is provided over the first electrode that a layer of
20 conducting material which forms a second electrode is provided over the first isolator, that a further layer of isolating material which forms a second isolator is provided over the second electrode, that a layer of conducting material which forms a third electrode is provided over the second isolator, said first and third electrode respectively comprising the drain and source
25 electrode of the transistor or vice versa and said second electrode the gate electrode of the transistor, that at least said second and said third electrode and said first and second isolator with the respective layers in stacked configuration form a step oriented vertically relative to said first electrode and/or said substrate, and that a semiconductor material which forms the
30 active semiconductor of the transistor is provided over the exposed portion of said first electrode, said second electrode and said third electrode, said active semiconductor contacting the gate electrode directly and forming a substantially vertically oriented transistor channel between said first and said third electrode and a metal-oxide semiconductor field-effect transistor
35 (MOSFET) which is characterized in that that a layer of conducting material which comprises a first electrode is provided on the substrate, that a layer of isolating material which forms a first isolator is provided over the first electrode, that a layer of conducting material which forms a second electrode

is provided over the first isolator, that a further layer of isolating material which forms a second isolator is provided over the second electrode, that a layer of conducting material which forms a third electrode is provided over the second isolator, said first and third electrode respectively comprising the
5 drain and source electrode of the transistor or vice versa and said second electrode the gate electrode of the transistor, that at least said second and said third electrode and said first and second isolator with the respective layers in stacked configuration form a step oriented vertically relative to said first electrode and/or said substrate, that a vertically oriented layer of
10 isolating material which forms a gate isolator is provided over said second electrode and on said vertical step, and that a semiconductor material which realizes the active semiconductor of the transistor and forms a substantial vertically oriented transistor channel between said first and said third electrode is provided over the exposed portion of said first electrode, said
15 vertical step with said gate isolator and said third electrode.

Further the above-mentioned objects and advantages according to the invention are achieved with a method for fabrication of a field-effect transistor, characterized by the method comprising steps for depositing on said substrate a layer of conducting material which forms a first electrode,
20 forming on the first electrode a step consisting of a photoresist and vertical relative to said first electrode and/or said substrate by means of a photolithographic process, depositing respectively over both said conducting layer and said photoresist which form the vertical step, a first isolator, a
25 conducting material which forms a second electrode, a second isolator and a conducting material which forms a third electrode in a layerwise stacked configuration, removing said configuration stacked over said photoresist and the photoresist itself by means of a lift-off method, whereby the remaining isolator-electrode configuration provided on the first electrode forms a step oriented vertically relative to said first electrode and/or said substrate, and
30 depositing a soluble amorphous active semiconductor material over said first electrode, and said vertical step, such that semiconductor material contacts both said first and said third electrode which realize respectively a drain or source electrode and vice versa in a field-effect transistor, and said second electrode which realizes the gate electrode of the field effect transistor, thus
35 forming a vertically oriented transistor channel.

When the field-effect transistor is a metal-oxide field-effect transistor (MOSFET) it is advantageous that an isolating material is being deposited on the vertical step in a vertically oriented layer, which is provided over the second electrode and forms the gate isolator in a field-effect transistor, the deposition taking place after the removal of said stacked configuration and said photoresist, but before the deposition of the soluble amorphous active semiconductor material.

It is according to the invention also advantageous that the active semiconductor material is an amorphous inorganic or organic semiconductor material, but need not be restricted to amorphous semiconductor materials, as it may also be selected among polycrystalline or microcrystalline inorganic or organic semiconductor materials.

Further features and advantages are apparent from the remaining appended dependent claims.

The invention shall now be discussed in greater detail with reference to the drawings wherein

- fig. 1a shows an example of prior art as mentioned above,
- fig. 1b another example of prior art as mentioned above,
- fig. 1c an example of a planar junction field-effect transistor according to prior art,
- fig. 2 a preferred embodiment of a junction field-effect transistor according to the invention,
- fig. 3 a preferred embodiment of a MOSFET according to the invention,
- fig. 4a-e the different process steps in an embodiment of the method according to the invention whereby the field-effect transistor is realized as a junction field-effect transistor, and
- fig. 5a, 5b further process steps in order to realize a MOSFET according to the invention.

Fig. 2 shows the embodiment of a junction field-effect transistor (JFET) according to the invention. It is wholly realized in thin-film technology, such as will be explained in more detail in the following. On a substrate 1 there is provided a layer 2 of a conducting material which forms a first electrode in the transistor. On this layer an isolating material 3a is provided which forms

a first isolator and over the first isolator 3a a further conducting material 4 is provided, for instance a metal which forms a second electrode 4 of the transistor. On the second electrode 4 an isolating material 3b is provided which forms a second isolator in the transistor and over the second isolator 3b a layer 5 of conducting material is provided which forms a third electrode in transistor.

Realized as a junction field-effect transistor the first electrode 2 and the third electrode 5 now respectively form the drain electrode and the source electrode of the transistor or vice versa. The second electrode 4 forms the gate electrode. Both the second and third electrode 4, 5 and the isolators 3a, 3b are provided on the first electrode 2 such that they against the first electrode 2 and the substrate 1 form a vertical step, the extension of which is indicated by the reference number 6 in fig. 2. Thus the structure consisting of the second and third electrode 4; 5 and the isolators 3 covers only a portion of the substrate 1 and the horizontal extension of the layers which form the vertical step 6 on the first electrode 2 or the substrate 1, may be made comparatively small.

A layer 8 of an active semiconductor material which may be an amorphous, polycrystalline or microcrystalline inorganic or organic semiconductor material, is provided over the top of the third electrode 5 which for instance may be the source electrode of the transistor, over the vertical step 6 and the exposed vertical surface of the gate electrode 4 which is included in the vertical step 6, and down to the first electrode 2. The gate electrode 2 and the semiconductor material 8 now form a pn junction. A substantially vertical transistor channel 9 is defined as either a p channel or a n channel in the active semiconductive material 8 and extends between the first electrode 2 and the third electrode 5 and substantially adjacent to a pn junction at the gate electrode 4. Realized in this manner, the structure shown in fig. 2 forms a junction field effect transistor (JFET). It may optionally be made with the first electrode 2 as drain electrode and the third electrode 5 as source electrode or vice versa. The transistor effect, in this case the effective size of the transistor channel, is controlled by an electric field which is applied to the transistor channel over the pn junction.

Fig. 3 shows the embodiment of a MOSFET according to the invention. It is wholly realized in thin-film technology, as will be explained in more detail in

the following. On a substrate 1 a layer 2 of conducting material is provided which forms a first electrode in the transistor. On this layer an isolating material 3a which forms a first isolator is provided and over the first isolator 3a a further conducting material is provided, for instance metal, which forms a second electrode in the transistor. On the second electrode 4 an isolating material 3b is provided which forms a second isolator in the transistor, and over the second isolator 3b a layer 5 of conducting material is provided which forms a third electrode of the transistor.

Realized as a MOSFET the first electrode 2 and the third electrode 5 now forms respectively the drain electrode and the source electrode of the transistor or vice versa. The second electrode 4 forms the gate electrode. Both the second and the third electrode 4,5 and isolators 3a, 3b are provided on the first electrode 2 such that they in relation to the first electrode 2 and the substrate 1 form a vertical step, the extension of which is indicated by the reference number 6 in fig. 2. Thus the structure consisting of the second and the third electrode 4,5 and the isolators 3 covers only a portion of the substrate 1 and the horizontal extension of the layers which form the vertical step 6 on the first electrode 2 or the substrate 1, may be made comparatively small.

Over the exposed vertical surface of the gate electrode 4 which is included in the vertical step 6, an isolating material 7 is provided which forms the gate isolator of the field-effect transistor. Over the top of the third electrode 5 which for instance may be the source electrode of the transistor, over the vertical step 6 and down to the first electrode 2 a layer of active semiconductor material is provided which may be an amorphous, polycrystalline or microcrystalline inorganic or organic semiconductor material. The gate electrode 4 is isolated against the active semiconductor material 8 by the gate isolator 7 such that charge injection is prevented. A substantially vertical transistor channel is defined in the active semiconductor material 8 and extends between the first electrode 2 and the third electrode 5 and substantially adjacent to the vertical step 6. Realized in this manner the structure shown in fig. 2 forms a metal-oxide semiconductor field-effect transistor (MOSFET). Optionally it may be made with a first electrode 2 as drain electrode and the third electrode 5 as source electrode or vice versa. The transistor effect will either be given by a depletion mode or an enrichment mode, depending on the gate potential.

It is to be understood that the substrate 1 in the embodiments in figs. 2 and 3 exclusively is intended to be a carrier of the transistor structure. Further the conducting layer 2 and the first electrode are provided over the whole substrate, i.e. unpatterned, but it may equally well be patterned and might then for instance cover a portion of the substrate corresponding to that covered by the vertical step structure. For instance may then the first electrode in the embodiment in fig. 2 flush with the surface of the vertical step 6 and itself present a vertical step in relation to the substrate 1. This vertical step may here for instance flush with the vertical surface of the gate isolator 7. It is, of course, a condition that the necessary contact to the active semiconductor material 8 is obtained. A first electrode with a vertical step in relation to the substrate may additionally be advantageous if the first electrode shall be connected galvanically with corresponding electrodes on other transistors in a transistor network. For this purpose an electric conductor may then be provided on the horizontal surface of the substrate beyond the vertical step.

Now a method for fabrication of a junction field-effect transistor in thin-film technology according to the invention shall be discussed in more detail with reference to figs. 4a-e. A central task in connection with the fabrication of junction field-effect transistors as shown in figs. 2 and 3 is the forming of the vertical step over which the transistor effect in its entirety will be present. For instance a so-called lift-off method may be used which has proved to be an effective method for forming a vertical surface.

It is to be understood that the different process steps which is shown in figs. 4a-e and which now shall be discussed, are rendered schematically and simplified.

As shown in fig. 4a a layer 2 of conductive material is deposited in a first process step on the substrate 1 which itself is made in an isolating or dielectric material. The conducting material 2 now will be forming the first electrode of the transistor. Above the conducting material 2 a photoresist is deposited and masked and etched according to well-known photolithographic procedures, such that a patterned photoresist layer 10 with a vertical step 11 is formed on the first electrode 2. This is shown in fig. 4b and comprises a second process step of the method. In a third process step shown in fig. 4c, the isolating layer 3a which forms the first isolator, a conducting material 4,

which forms the second electrode of the transistor, a second isolating layer 3b which forms the second isolator, and on the top thereof a layer 5 of conducting material which forms a third electrode of the transistor are provided sequentially. By using for instance a vapour deposition process the layers 3,4,5 now will cover both the exposed portion of the first electrode 2 and the top of the photoresist 10 in horizontally stacked layers, such as evident from fig. 4c.

In a fourth process step a lift-off method is now used for removing the layer on the top of the photoresist and the photoresist 10 itself. This is done by means of a solvent process, for instance with acetone. When the photoresist 10 and the layers on the top thereof are removed, the component appears as shown in fig. 4d after the fourth process step and with a step 6 vertically oriented relative to the first electrode 2 or the substrate 1.

Then a soluble amorphous active semiconductor material 8 is deposited over the first electrode 2, the second electrode 4 and the vertical step 6 and the top surface of the third electrode 5 in a fifth process step shown in fig. 4e. The active semiconductor 8 thus will cover the layer structures both horizontally and vertically. In case the first electrode 2 is patterned and only covers a portion of the substrate 1, for instance such that it itself forms a vertical step which is flush with the vertical step 6, there will in addition neither be a problem with the contact between the first electrode 2 and the active semiconductor material 8.

In the fabrication of a MOSFET in thin-film technology according to the invention an intermediate process step shown in fig. 5a is applied after the fourth process step shown in fig. 4d. In this further process step an isolating layer 6 is provided over the second electrode 4 such that the surface thereof is covered in the vertical step 6. This isolating layer 7 now comprises the gate isolator of the MOSFET and prevents charge injection. The gate isolator 7 may be made in a process where an oxide is provided with the first electrode 2 as substrate. Then a vertical etching step is used for forming the gate isolator 7 oriented in the vertical direction such that it covers the gate electrode 4. Alternatively the gate isolator 7 also could be provided by making the gate electrode 4 in a material which may be oxidized selectively or processed in one way or another such that an isolating layer is formed on

the surface of the gate electrode. Preferably this may take place by selective oxidation of the material in the surface of the gate electrode 4.

After having provided the gate isolator 7 in the further process step shown in fig. 5a, the soluble amorphous active semiconductor material 8 is applied
5 over the first electrode 2, the gate isolator 7, the vertical step 6, and the top surface of the third electrode 5 in the process step shown in fig. 5b. This process step corresponds to the fifth process step shown in fig. 4e. The active semiconductor material thus will cover the layer structures both horizontally and vertically. In case the first electrode 2 is patterned and covers only a
10 portion of the substrate 1, but such that it extends somewhat beyond the vertically stacked layers, there will in addition be no problem with the contacting between the first electrode 2 and the active semiconductor material 8.

For the application of the amorphous active semiconductor material 8
15 methods like vacuum sublimation, vacuum deposition, spin coating and casting from solutions may be used. This implies that the amorphous active semiconductor material 8 in principle may be made with various structures which for instance cover the gate electrode 4 with different orientation both vertically and horizontally. It is also to be understood that the various active
20 materials may be mixed or combined in the amorphous semiconductor material in order to provide the field-effect transistor with special functions. If the field-effect transistor is a JFET, it may particularly be desired to use materials which spontaneously form a Schottky junction with the gate electrode, such that a MESFET structure is obtained.

25 Even if the fabrication of the field-effect transistors according to the invention in figs. 2 and 3 is shown for an in principle discrete component, there is nothing against fabricating transistors of this kind and with the method used in semi- or full- continuous reel-to-reel processes with global layer application. The active semiconductor material 8 may in this way be
30 applied in a continuous process. Correspondingly, also the gate isolator may in this way be applied in a continuous process if the field-effect transistor is a MOSFET. In a continuous process the vertical step 6 then advantageously will be formed parallel with the movement direction of the line and both the gate isolator 7 and the active semiconductor material may be applied as
35 continuous strips on the vertical step. After the last process step shown in fig.

4e Fig. 5b, the individual transistors may be separated from the line and completed in the form of discrete components.

5 However, there is nothing against that greater portions of the line with a large number of transistors may form a transistor array which in its turn may be used for realizing active memory modules with the individual transistor as a memory element. The transistor must then be connected in a galvanic network by forming suitable conducting structures for the connections.

10 Generally vertical field-effect transistor as disclosed herein may be realized as structural parts in integrated electronic circuits in two and three dimensions. Possible applications of such circuits may be memories, processors etc. An obvious advantage of using active memory components based on transistors according to the present invention is the possibility of writing in small-signal mode and reading in large-signal mode, which particularly will be an advantage in electrical addressing of memory locations
15 in large memory modules realized in a matrix network.

In regard of the fabrication process for the field-effect transistors according to the invention, it may as mentioned be realized globally by using continuous lines. In such a case it will also be possible to fabricate field-effect transistors as JFET and MOSFET with a vertical geometric
20 structure by means of a printing method and not only by using well-known fabrication processes for VLSI components.

PATENT CLAIMS

1. A field-effect transistor, particularly a junction field-effect transistor (JFET) with substantially vertical geometry, wherein the transistor comprises a planar substrate (1) of non-conducting material,
5 characterized in that a layer (2) of conducting material which comprises a first electrode is provided on the substrate (1), that a layer (3a) of isolating material which forms a first isolator is provided over the first electrode (2), that a layer of conducting material (4) which forms a second electrode is provided over the first isolator (3a), that a further layer (3b) of isolating
10 material which forms a second isolator is provided over the second electrode (4), that a layer (5) of conducting material which forms a third electrode is provided over the second isolator (3b), said first (2) and third electrode (5) respectively comprising the drain and source electrode of the transistor or vice versa and said second electrode (4) the gate electrode of the transistor,
15 that at least said second (4) and said third electrode (5) and said first (3a) and second isolator (3b) with the respective layers in stacked configuration form a step (6) oriented vertically relative to said first electrode (2) and/or said substrate (1), and that a semiconductor material (8) which forms the active semiconductor of the transistor is provided over the exposed portion of said
20 first electrode (2), said second electrode (4) and said third electrode (5), said active semiconductor (8) contacting the gate electrode (4) directly and forming a substantially vertically oriented transistor channel (9) between said first (2) and said third electrode (5).
2. A field-effect transistor, particularly a metal-oxide semiconductor
25 field-effect transistor (MOSFET) with substantially vertical geometry, wherein the transistor comprises a planar substrate (1) of non-conducting material, characterized in that a layer (2) of conducting material which comprises a first electrode is provided on the substrate (1), that a layer (3a) of isolating material which forms a first isolator is provided over the first
30 electrode (2), that a layer of conducting material (4) which forms a second electrode is provided over the first isolator (3a), that a further layer (3b) of isolating material which forms a second isolator is provided over the second electrode (4). that a layer (5) of conducting material which forms a third electrode is provided over the second isolator (3b), said first (2) and third
35 electrode (5) respectively comprising the drain and source electrode of the

transistor or vice versa and said second electrode (4) the gate electrode of the transistor, that at least said second (4) and said third electrode (5) and said first (3a) and second isolator (3b) with the respective layers in stacked configuration form a step (6) oriented vertically relative to said first electrode (2) and/or said substrate (1), that a vertically oriented layer (7) of isolating material which forms a gate isolator is provided over said second electrode (4) and on said vertical step (6), and that a semiconductor material (8) which realizes the active semiconductor of the transistor and forms a substantial vertically oriented transistor channel (9) between said first (2) and said third electrode (5) is provided over the exposed portion of said first electrode (2), said vertical step (6) with said gate isolator (7) and said third electrode (5).

3. A field-effect transistor according to claim 1 or claim 2, characterized in that the first electrode (2) is provided patterned on the substrate (1) and forms a further intermediate step relative to the substrate (1), whereby every electrode (2, 4, 5) presents a substantially vertical surface to the active semiconductor (8).

4. A field-effect transistor according to claim 1 or claim 2, characterized in that the semiconducting material (8) is selected among amorphous, polycrystalline or microcrystalline inorganic or organic semiconductor materials.

5. A field-effect transistor according to claim 1 or claim 2, characterized in that the transistor channel (9) is defined as the vertical portion of the active semiconductor (8) between said first (2) and said third electrode (5) and adjacent to the vertical step (6) formed by the stacked configuration.

6. A field-effect transistor according to claim 1, characterized in that the semiconducting material (8) and the gate electrode (4) spontaneously form a Schottky junction (7).

7. A field-effect transistor according to claim 1, characterized in that the transistor channel (9) is defined as an n channel or p channel in the vertical portion of the active semiconductor (8) between said first (2) and second electrode (5) and adjacent to a pn junction at the gate electrode (4).

8. A field-effect transistor according to claim 2, characterized in that the gate isolator (7) is formed as an oxide coating on the vertical surface of the gate electrode (5).

9. A field-effect transistor according to claim 8, characterized in that the oxide coating (7) is formed by selective oxidation of the electrode material in the surface of the gate electrode (4).

10. A method for fabrication of a field-effect transistor with substantially vertical geometry, wherein the transistor comprises a planar substrate (1) of non-conducting material, characterized by the method comprising steps for depositing on said substrate (1) a layer (2) of conducting material which forms a first electrode, forming on the first electrode (2) a step (6) consisting of a photoresist (10) and vertical relative to said first electrode (2) and/or said substrate (1) by means of a photolithographic process, depositing respectively over both said conducting layer (2) and said photoresist (10) which form the vertical step (6), a first isolator (3a), a conducting material (4) which forms a second electrode, a second isolator (3b) and a conducting material (5) which forms a third electrode in a layerwise stacked configuration, removing said configuration stacked over said photoresist (10) and the photoresist itself by means of a lift-off method, whereby the remaining isolator-electrode configuration provided on the first electrode (2) forms a step (6) oriented vertically relative to said first electrode (2) and/or said substrate (1), and depositing a soluble amorphous active semiconductor material over said first electrode (2), and said vertical step (6), such that semiconductor material contacts both said first (2) and said third electrode (5) which realize respectively a drain or source electrode and vice versa in a field-effect transistor, and said second electrode (4) which realizes the gate electrode of the field effect transistor, thus forming a vertically oriented transistor channel (9).

11. A method according to claim 10, wherein the field-effect transistor is a metal-oxide semiconductor field-effect transistor (MOSFET), characterized by an isolating material being deposited on the vertical step (6) in a vertically oriented layer, which is provided over the second electrode (5) and forms the gate isolator in a field-effect transistor, the deposition taking place after the removal of said stacked configuration and said photoresist (10), but before the deposition of the soluble amorphous active semiconductor material (8).

12. A method according to claim 11, characterized by the gate isolator (7) being formed as an oxide coating on the vertical surface of the gate electrode (4).

5 13. A method according to claim 12, characterized by the oxide coating (7) being formed by selective oxidation of the electrode material in the surface of the gate electrode (4).

14. A method according to claim 10, characterized by the first electrode (2) being deposited patterned on the substrate (1) and covering only partially the latter.

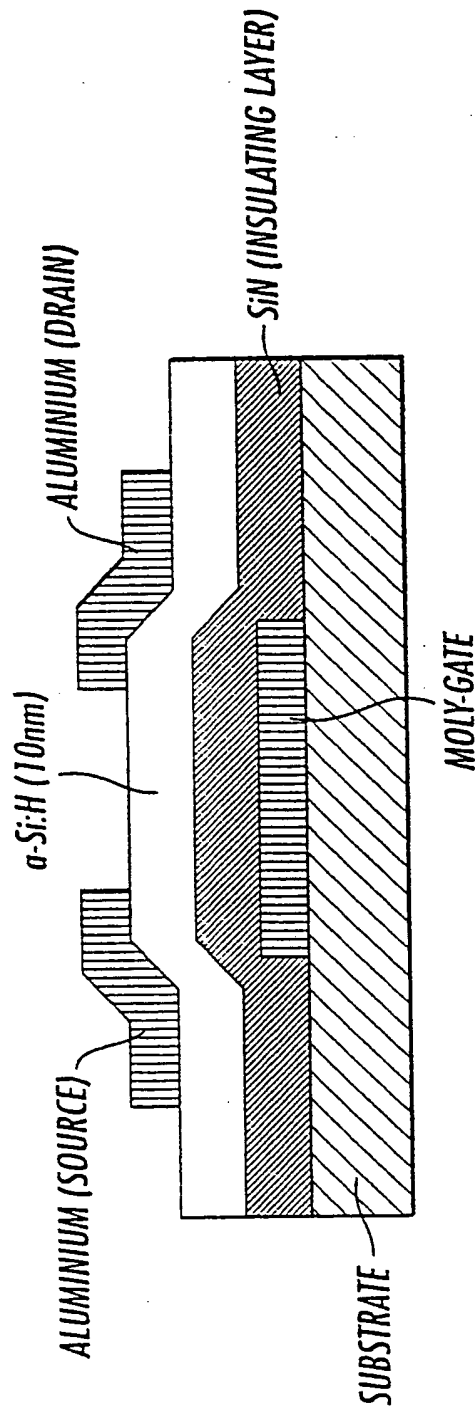


Fig. 1a STRUCTURE OF AN α -Si:H THIN FILM TRANSISTOR

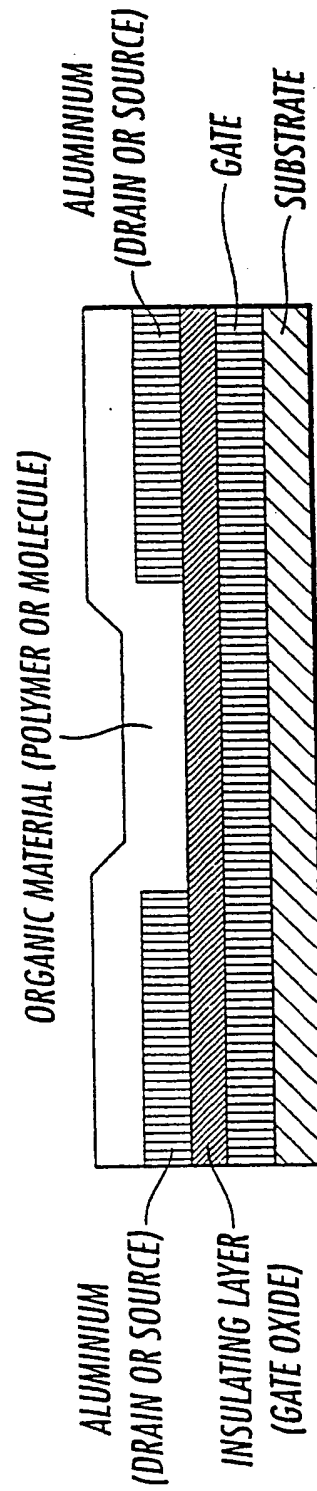


Fig. 1b STRUCTURE OF A ORGANIC THIN FILM TRANSISTOR

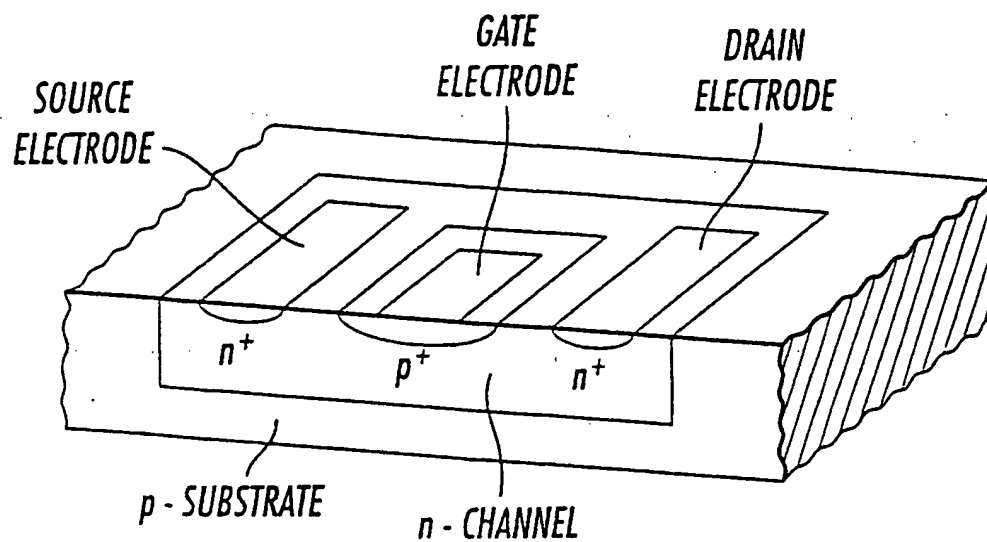


Fig. 1c

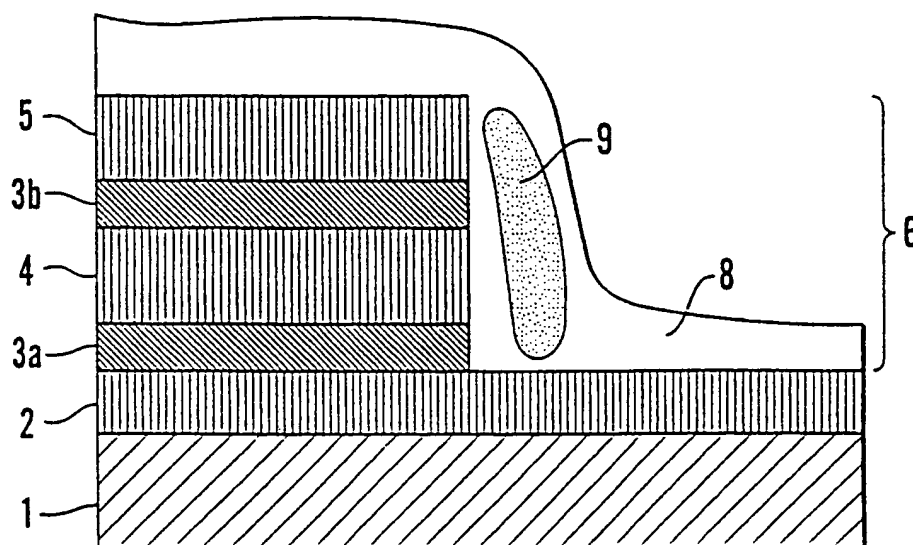


Fig. 2

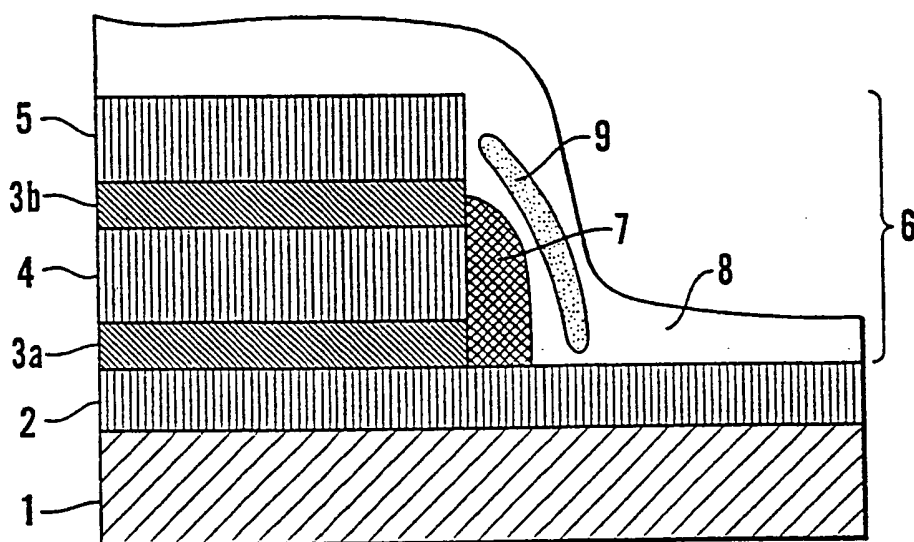


Fig.3

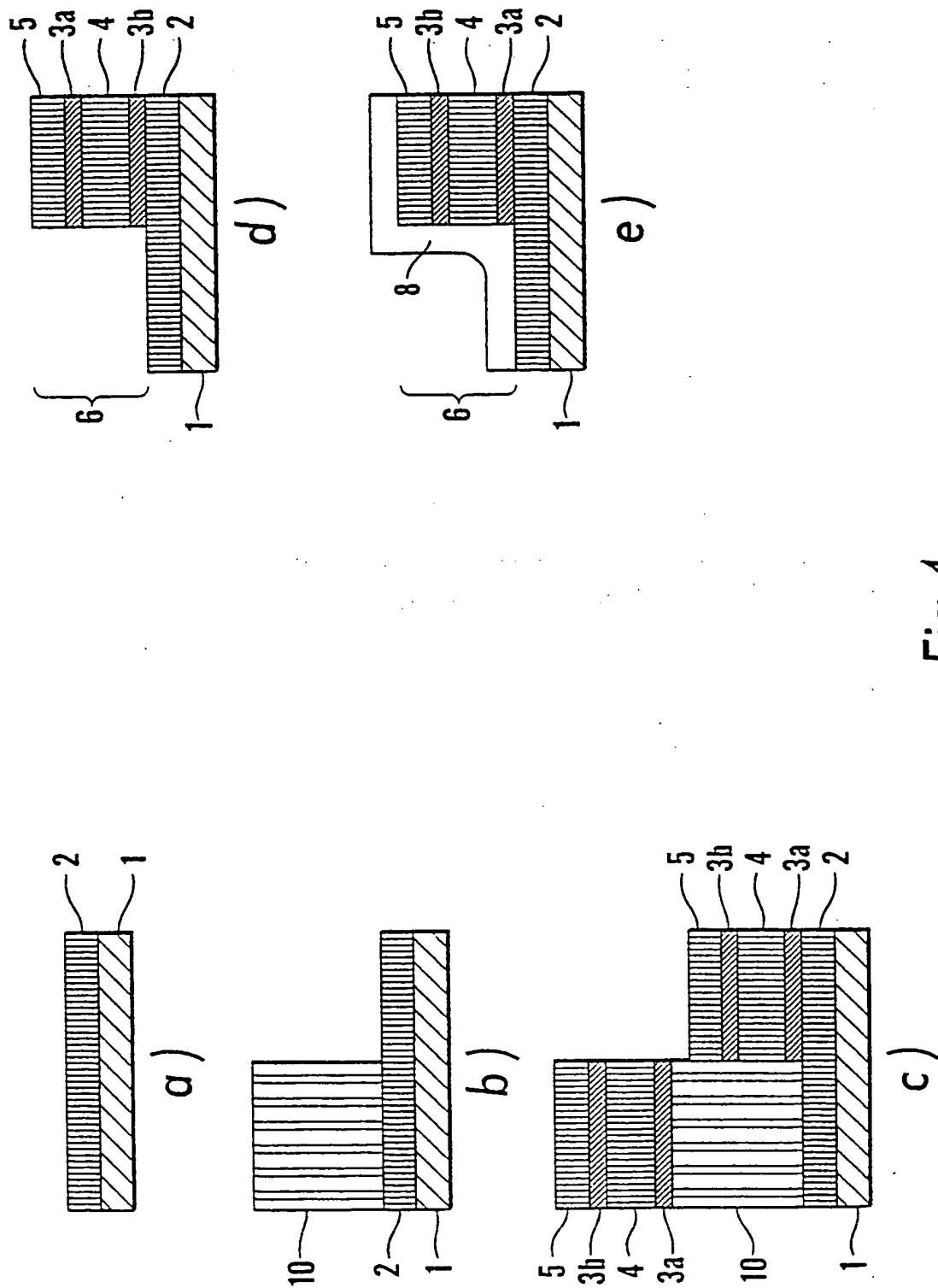


Fig. 4

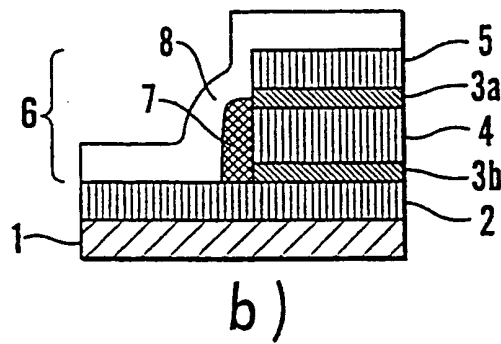
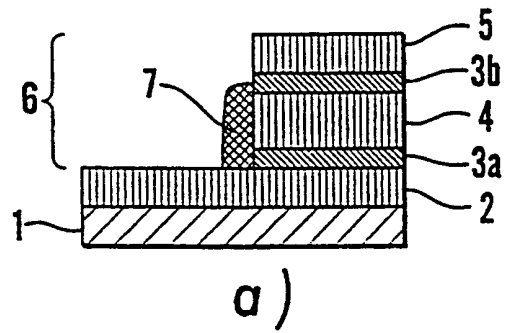


Fig.5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/NO 99/00013

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 29/772, H01L 21/335, H01L 51/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EDOC, WPIL, JAPIO, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4677451 A (JAMES D. PARSONS ET AL), 30 June 1987 (30.06.87), column 3, line 57 - column 7, line 45	1,4,5,6
A	--	7-13
X	US 4735918 A (JAMES D. PARSONS ET AL), 5 April 1988 (05.04.88), column 3, line 58 - column 7, line 46	1,4,5,6
A	--	7-13
A	US 5047812 A (JAMES R. PFIESTER), 10 Sept 1991 (10.09.91), see whole document	2,4-13
	--	



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

21 June 1999

Date of mailing of the international search report

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,A	US 5780911 A (JOON YOUNG PARK ET AL), 14 July 1998 (14.07.98), see whole document --	1-13
A	US 4587540 A (THOMAS N. JACKSON), 6 May 1986 (06.05.86), see whole document -- -----	1,4-13

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/NO 99/00013

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4677451 A	30/06/87	US 4735918 A	05/04/88
US 4735918 A	05/04/88	US 4677451 A	30/06/87
US 5047812 A	10/09/91	NONE	
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		JP 9232448 A	05/09/97
US 4587540 A	06/05/86	EP 0091548 A,B	19/10/83
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		JP 63023669 B	17/05/88

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